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1 Cluster reserves: a mechanism for resource management in cluster-based network server:



Mohit Aron, Peter Druschel, Willy Zwaenepoel

June 2000

ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 2000 / SIGMETRICS international conference on Measurement and modeling of comp systems SIGMETRICS '00, Volume 28 Issue 1

Publisher: ACM Press

Full text available: pdf(975.49 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index te](#)

In network (e.g., Web) servers, it is often desirable to isolate the performance of different class from each other. That is, one seeks to achieve that a certain minimal proportion of server resou available for a class of requests, independent of the load imposed by other requests. Recent wo demonstrates how to achieve this performance isolation in servers consisting of a single, centra however, achieving performance isolation in a distributed, cluster bas ...

2 Focus on the Asanté FriendlyNET FR1104-G router

Gilbert Held

November 2004 **International Journal of Network Management**, Volume 14 Issue 6

Publisher: John Wiley & Sons, Inc.

Full text available: pdf(341.23 KB)

Additional Information: [full citation](#), [index terms](#)

3 A simple linear model of demand paging performance



Jerome H. Saltzer

April 1974

Communications of the ACM, Volume 17 Issue 4

Publisher: ACM Press

Full text available: pdf(615.52 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index te](#)

Predicting the performance of a proposed automatically managed multilevel memory system rec model of the patterns by which programs refer to the information stored in the memory. Some experimental measurements on the Multics virtual memory suggest that, for rough approximati remarkably simple program reference model will suffice. The simple model combines the effect information reference pattern with the effect of the automatic management algorithm to produc

Keywords: Multics, associative memory, demand paging, memory models, memory usage acc multilevel memory systems, paging, performance measurement, program models, virtual mem

4

Architectural walkthroughs using portal textures

Daniel G. Aliaga, Anselmo A. Lastra

October 1997 **Proceedings of the 8th conference on Visualization '97**

Publisher: IEEE Computer Society Press

Full text available:  [pdf\(980.76 KB\)](#) 
[Publisher Site](#)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)


5 Continuous contact simulation for smooth surfaces



Paul G. Kry, Dinesh K. Pai

January 2003 **ACM Transactions on Graphics (TOG)**, Volume 22 Issue 1

Publisher: ACM Press

Full text available:  [pdf\(1.52 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Dynamics simulation of smooth surfaced rigid bodies in contact is a critical problem in physically animation and interactive virtual environments. We describe a technique that uses reduced coordinate evolution to evolve a single continuous contact between smooth piecewise parametric surfaces. The incorporation of friction into our algorithm is straightforward. The dynamics equations, although slightly more complex than the reduced coordinate formulation, can be integrated easily using explicit in ...

6 Energy efficient microarchitectural techniques: Energy-efficient instruction set synthesis for specific processors



Jong-eun Lee, Kiyoung Choi, Nikil D. Dutt

August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Publisher: ACM Press

Full text available:  [pdf\(78.03 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Several techniques have been proposed to enhance the energy-efficiency of ASIPs (Application-Specific Instruction Set Processors). While those techniques can reduce the energy consumption with a change in the instruction set (IS), they fail to exploit the opportunity of designing the entire IS from an energy-efficiency perspective. In this paper, we present an energy-efficient IS synthesis technique that comprehensively reduce the energy-delay product (EDP) of ASIPs through optimal ...

Keywords: application-specific instruction set processor (ASIP), customization, energy-delay product, instruction encoding, low power

7 Session 7: rendering: Interruptible rendering



Cliff Woolley, David Luebke, Benjamin Watson, Abhinav Dayal

April 2003 **Proceedings of the 2003 symposium on Interactive 3D graphics**

Publisher: ACM Press

Full text available:  [pdf\(13.15 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Interruptible rendering is a novel approach to the fidelity-versus-performance tradeoff ubiquitous in interactive rendering. Interruptible rendering unifies spatial error caused by rendering coarse approximations and temporal error caused by the delay imposed by rendering into a single image-space error metric. The heart of this approach is a progressive rendering framework that renders a coarse image into the final image and continuously refines it while monitoring temporal error. When ...

Keywords: level of detail, mesh simplification, perceptually motivated rendering


8 GraalBench: a 3D graphics benchmark suite for mobile phones



Iosif Antochi, Ben Juurlink, Stamatios Vassiliadis, Petri Lohja

June 2004 **ACM SIGPLAN Notices , Proceedings of the 2004 ACM SIGPLAN/SIGBED conference on Programming Languages, compilers, and tools for embedded systems LCTES '04**, Volume 39 Issue 6

Publisher: ACM Press

Full text available:  [pdf\(439.20 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

In this paper we consider implementations of embedded 3D graphics and provide evidence indicating their suitability for mobile phones.

benchmarks employed for desktop computers are not suitable for mobile environments. Consequently we present GraalBench, a set of 3D graphics workloads representative for contemporary and emerging devices. In addition, we present detailed simulation results for a typical rasterization pipeline. To show that the proposed benchmarks use only a part of the resources offered by c ...

Keywords: 3D graphics benchmarking, embedded 3D graphics architectures

9 Digital circuits design: Design of a decompressor engine on a SPARC processor



E. Billo, R. Azevedo, G. Araujo, P. Centoducatte, E. Wanderley Netto

September 2005 **Proceedings of the 18th annual symposium on Integrated circuits and systems SBCCI '05**

Publisher: ACM Press

Full text available: pdf(130.36 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Code compression, initially conceived as an effective technique to reduce code size in embedded systems, today also brings advantages in terms of performance and energy consumption, due to an increased cache hit ratio. This paper proposes the design of a code decompressor engine for our dictionary-based method, embedding it into the Leon (SPARC V8) processor. Our design guarantees that the processor time is maintained and the decompression is performed on-the-fly. We have achieved a ...

Keywords: code compression, performance

10 The Mahler experience: using an intermediate language as the machine description



David W. Wall, Michael L. Powell

October 1987 **ACM SIGARCH Computer Architecture News , ACM SIGPLAN Notices , ACM SIGOPS Operating Systems Review , Proceedings of the second international conference on Architectural support for programming languages and operating systems ASP**
Volume 15 , 22 , 21 Issue 5 , 10 , 4

Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(618.75 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Division of a compiler into a front end and a back end that communicate via an intermediate language is a well-known technique. We go farther and use the intermediate language as the official description of machines with simple instruction sets and addressing capabilities, hiding some of the inconveniences of the real machine from the users and the front end compilers. To do this credibly, we have had to consider not only the existence of the details but also the performance consequences ...

11 Session A: Computer graphics: Implementation and applications of the distortion operator



Shaun Bangay

November 2001 **Proceedings of the 1st international conference on Computer graphics, virtual reality and visualisation**

Publisher: ACM Press

Full text available: pdf(1.09 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The distortion operator transforms 2D images in a manner similar to image warping or morphing, allowing source pixels to be mapped to any destination pixel. This operator can be implemented on current hardware allowing at least one distortion per frame at interactive frame rates. Potential applications are numerous. Those described include re-mapping images for correct projection onto curved screens, correcting perspective distortion from multiple sources simultaneously, and allowing constant time ...

Keywords: MMX, image warping, lighting, projection, texturing

12 Mobility, Modeling, and Management: Performance analysis of optimized smooth handoff in wireless networks



C. Blondia, N. Van den Wijngaert, G. Willems, O. Casals

September 2002 **Proceedings of the 5th ACM international workshop on Modeling analysis and simulation of wireless and mobile systems**

Publisher: ACM Press

Full text available: pdf(1.20 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Mobile IP allows node mobility involving changes of point-of-attachment to the Internet. In order to reduce the impact on the performance and the signaling overhead, hierarchical mobility management schemes have been introduced. These schemes define protocols that allow movements within a domain to be handled locally, without involvement of the mobile node's home network. In order to reduce more the ping-pong during handoff, new schemes have been defined, such as smooth handoff. By storing p ...

Keywords: OPNET, analytical modelling, micro mobility management, mobile IP, performance : smooth handoff

13 Correlation and aliasing in dynamic branch predictors



Stuart Sechrest, Chih-Chieh Lee, Trevor Mudge

May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture ISCA '96**, Volume 24 Issue 2

Publisher: ACM Press

Full text available: [pdf\(1.60 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Previous branch prediction studies have relied primarily upon the SPECint89 and SPECint92 benchmarks for evaluation. Most of these benchmarks exercise a very small amount of code. As a consequence, resources required by these schemes for accurate predictions of larger programs have not been evaluated. Moreover, many of these studies have simulated a very limited number of configurations. Here we present simulations of a variety of branch prediction schemes using a set of relatively large benchmarks ...

14 An empirical study of conservative scheduling

Ha Yoon Song, Richard A. Meyer, Rajive Bagrodia

May 2000 **Proceedings of the fourteenth workshop on Parallel and distributed simulation**

Publisher: IEEE Computer Society

Full text available: [pdf\(739.52 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

It is well known that the critical path provides an absolute lower bound on the execution time of conservative parallel discrete event simulation. It stands to reason that optimal execution time can be achieved by immediately executing each event on the critical path. However, dynamically identifying the critical event is difficult, if not impossible. In this paper, we examine several heuristics that might determine the critical event, and conduct a performance study ...

15 Scheduling critical channels in conservative parallel discrete event simulation

Z. Xiao, B. Unger, R. Simmonds, J. Cleary

May 1999 **Proceedings of the thirteenth workshop on Parallel and distributed simulation**

Publisher: IEEE Computer Society

Full text available: [pdf\(727.14 KB\)](#)

[Publisher Site](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper introduces the Critical Channel Traversing (CCT) algorithm, a new scheduling algorithm for sequential and parallel discrete event simulation. CCT is a general conservative algorithm that is suitable for the simulation of low-granularity network models on shared-memory multi-processor computers. The implementation of the CCT algorithm within a kernel called TaskIt has demonstrated excellent performance for large ATM network simulations when compared to previous sequential, optimistic and ...

Keywords: ATM network modeling, parallel simulation, conservative PDES, optimistic PDES, Chandy-Bryant algorithm, time parallelism, Critical Channel Traversing algorithm.

16 Rendering with coherent layers



Jed Lengyel, John Snyder

August 1997 **Proceedings of the 24th annual conference on Computer graphics and interactive techniques**

Publisher: ACM Press/Addison-Wesley Publishing Co.

Full text available: [pdf\(1.32 MB\)](#)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

Keywords: Talisman, affine transformation, image compositing, image-based rendering, sprite

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